

DC-725 GHz Sampling Circuits and Subpicosecond Nonlinear Transmission Lines Using Elevated Coplanar Waveguide

U. Bhattacharya, S. T. Allen, and M. J. W. Rodwell

Abstract—Nonlinear transmission lines (NLTL's) fabricated with Schottky diodes on GaAs were used to electrically generate 3.7-V step functions that had a measured 10%–90% fall time of 0.68 ps. These NLTL's were integrated on wafer with sampling circuits that had a measured 3-dB bandwidth of 725 GHz. Key to circuit performance are the use of low-loss, high-wave-velocity elevated coplanar waveguide transmission lines and the elimination of active device pad parasitics by contacting devices above the plane of the wafer.

I. INTRODUCTION

NONLINEAR transmission lines (NLTL's) integrated with sampling circuits have been used in a variety of millimeter wave and submillimeter wave instruments [1]–[7]. In order to increase circuit bandwidth to beyond 500 GHz, high frequency limitations imposed by the coplanar waveguide transmission lines and interconnect parasitics were overcome. The circuit performance is then limited by the speed of the Schottky varactor diodes.

An NLTL is an electrical step function generator consisting of a high-impedance transmission line periodically loaded with varactor diodes [7]. The NLTL per-diode propagation delay $T_{\text{delay}} = [L_{\text{line}} \cdot (C_{\text{line}} + C_{\text{diode}}(V))]^{1/2}$ is a function of the diodes' capacitance, and both decrease with increasing reverse bias voltage. The falling edge of the waveform becomes steeper during propagation since the delay for the waveform peak is greater than for the trough. A shock wave is formed whose transition time is limited by the diodes' cutoff frequency $f_c = (2\pi R_d C_d)^{-1}$ and the Bragg frequency $f_{\text{Br}} = (\pi \cdot T_{\text{delay}})^{-1}$ that arises from the NLTL's periodicity.

To make f_{Br} high, the diode separation must be decreased, and the line's transverse dimensions proportionally reduced. This results in three difficulties as f_{Br} is increased to ≥ 1 THz. Decreasing the line's transverse dimensions results in conductors of 1–2 μm width having very large skin-effect losses. To make f_{Br} high the diode separation must be decreased, but this spacing is limited by the diodes' physical size. Most importantly, for small diode separations the diodes' pad parasitics on the GaAs surface contribute a large fraction

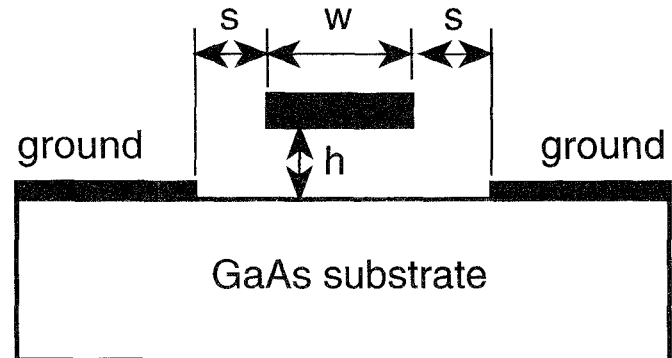


Fig. 1. Cross-section view of elevated coplanar waveguide. For the smallest geometry used in this work, $h = 3 \mu\text{m}$, $w = 8 \mu\text{m}$ and $s = 5 \mu\text{m}$. The transmission line's microwave parameters were $Z_0 = 76 \Omega$, and $v = 2.2 \cdot 10^8 \text{ m/s}$.

of C_{line} and hence both lower f_{Br} and decrease the change of T_{delay} with voltage.

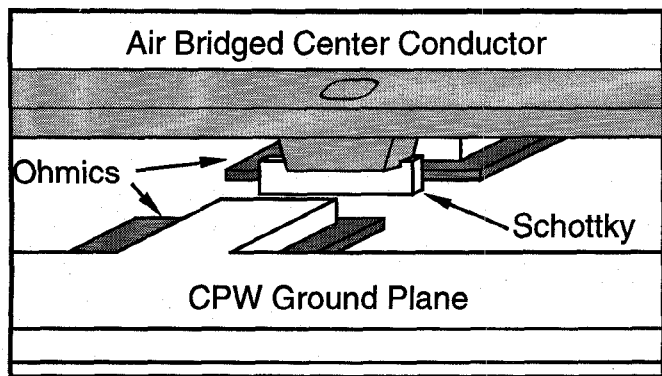
Normal air-bridge fabrication processes can be used to fabricate coplanar waveguide (CPW) transmission lines with the center conductor elevated 2–3 μm above the high- ϵ GaAs substrate (Fig. 1). The wave velocity is doubled and, hence, for the same physical separation between diodes, f_{Br} is doubled. In addition, because of the lower capacitance per unit length, the center conductor is wider for the same line impedance and hence the skin effect losses are reduced. Elevated CPW lines have been used to reduce loss at the NLTL input [4], where f_{Br} is low, but the large dimensions of the air-bridge post prevent the use of air bridges near the NLTL output, where the diode spacings are small. It is at the NLTL output, with its small diode spacings, very high skin-effect losses, and high f_{Br} , where elevated CPW is most needed.

We have fabricated NLTL's using a top-contacted elevated coplanar waveguide (Fig. 2). In this process, electrical contact between active devices (diodes) and transmission lines are made in air, above the plane of the wafer. As the interconnects are elevated coplanar waveguide, line losses are reduced and required diode spacings for a given f_{Br} increased. In addition, with the top-contacted technology, the diode's pad parasitics are eliminated, and the process alignment tolerances permit diode spacings as small as 15 μm and f_{Br} as high as 3 THz. While this paper addresses NLTL's, issues of CPW losses, CPW velocity, pad parasitics, and minimum feasible

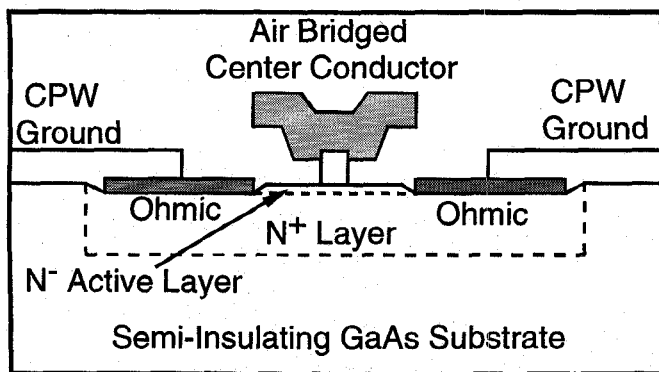
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(a)



(b)

Fig. 2. (a) Perspective view showing the elevated center conductor contacting the top of a diode. The Schottky contact was kept well away from the edge of the H^+ implanted region, which ends $2\ \mu\text{m}$ outside the ohmic contacts. (b) Cross-section at the plane of a diode.

transmission-line length will be relevant to any submillimeter-wave integrated circuit operating near or above 1 THz.

The process flow consists of forming ohmic contacts, ion implanting to provide isolation, depositing metal for the Schottky contacts and CPW ground planes, and then applying a layer of polyimide. The polyimide is subsequently etched in an O_2 R.I.E. system until $\approx 0.2\ \mu\text{m}$ of the Schottky metal is exposed. The posts for the elevated lines are formed on top of the polyimide and provide the contacts to the tops of the diodes. After electroplating the elevated lines, the polyimide is removed, leaving the contacts between the CPW and the diodes in air, substantially reducing the parasitic capacitance (Fig. 2).

By contacting the diodes this way, a small Schottky contact can be placed in the middle of a larger active region because the active area of the diode is defined by the footprint of the Schottky metal. The regions outside the active areas are H^+ implanted to render them semi-insulating, and the transverse straggle of the ions damages the active regions near the mask edge. By contacting the diodes from the top, $1\ \mu\text{m} \times 1\ \mu\text{m}$ sampling diodes were fabricated that suffered no performance degradation from H^+ the transverse straggle, as determined by DC measurements of the diode capacitance and forward-bias series resistance.

The NLTL's were designed to have $f_{\text{Br}} = 1500\ \text{GHz}$ and the $1\text{-}\mu\text{m}$ diodes on GaAs with an active layer of

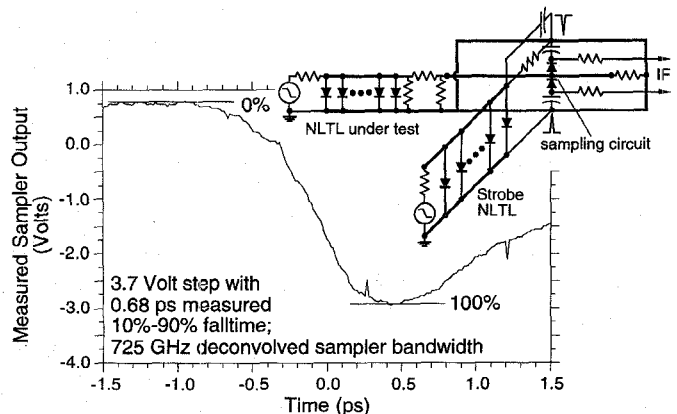


Fig. 3. Measured output from the sampling circuit integrated on wafer with two NLTL's showing the 0.68-ps step function. The inset shows a schematic diagram of the circuit.

$N_D = 1.10^{17}\ \text{cm}^{-3}$ had a large signal cutoff frequency $f_c = \text{THz}$ [3]. NLTL's providing separate strobe and test signals were integrated with sampling circuits to provide for on-wafer measurements (inset of Fig. 3). The bandwidth of the sampling circuits is determined by the aperture time of the strobe pulse and the 10%-90% RC charging time of the sampling diodes, both of which were $< 0.2\ \text{ps}$.

The measured waveform from the output of the sampler had a 3.7 V step with a 0.68-ps 10%-90% falltime (Fig. 3). In previous work, where the time constants of the sampling circuits and the NLTL's were comparable [3], [7], a simple sum-of-squares deconvolution has been used to determine the sampler bandwidth. Using that method here gives a conservative estimate for the sampler bandwidth of 725 GHz.

In the NLTL's varactor diodes at the output end of the line, the depletion edge was moving 145 nm in 0.68 ps, giving an average velocity of $2.1 \cdot 10^7\ \text{cm/sec}$. Because all other time constants in the circuit were much lower than this, the velocity saturation, which has been analyzed by others [8], appears to be the limiting phenomenon. $v_{\text{sat}} \approx 2 \cdot 10^7\ \text{cm/sec}$ has also been inferred from conversion-efficiency measurements of submillimeter-wave varactor diode frequency multipliers [9]. To overcome this limitation, heavier doping in the diodes can be used so that for the same voltage swing the distance the depletion edge must travel is reduced.

In summary, an elevated coplanar waveguide technology was developed that addresses problems that are generic to submillimeter wave integrated circuits: high skin effect losses and extremely short wavelengths. This technology was applied to NLTL's and the result was an integrated sampling circuit that had a 3 dB bandwidth of 725 GHz. The limitations to the circuit are now semiconductor device phenomena, and future investigations will address these issues.

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